AMENDMENTS TO THE SPECIFICATION

Please amend the third full paragraph on page 8 as follows:

~~The present invention provides a method and an apparatus that adds grant information to a memory that is used to grant access to a bus to insure that lower priority data streams are able to transmit information across the bus. The memory has a plurality of physical addresses where each physical address identifies an arbitration period.~~ A method of adding grant information to a memory that stores information about a series of arbitration periods is disclosed in accordance with a first embodiment of the present invention. The method includes assigning a number of first addresses to a group of devices such that two or more consecutive first addresses are assigned to each device and no two devices have the same first addresses. The number of first addresses represents a corresponding number of arbitration periods such that each first address represents one arbitration period. Each first address has a sequence of bits. The method also includes forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address and each second address has a corresponding device by rearranging the sequence of bits in a plurality of the number of first addresses. Each second address represents one arbitration period.

Please amend the fourth full paragraph on page 8 as follows:

~~The method of the present invention includes the step of, if grant information is to be added to the memory, determining a number of desired arbitration periods requested by a communication circuit. The method also includes the step of assigning a range of logical addresses to the communication circuit. The number of logical addresses in the range is equal to the number of desired arbitration periods.~~ A method of adding grant information to a memory that stores information about a series of arbitration periods is disclosed in accordance with a second embodiment of the present invention. The method includes assigning a number of first addresses to a device. The number of first addresses represents a corresponding number of arbitration periods such that each first address represents one arbitration period. Each first address has a sequence of bits. The method also includes forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address by rearranging the sequence of bits in a plurality of the number of first addresses. The first addresses and second addresses have an equal number of bits. Each second address represents one arbitration period.

Please amend the fifth paragraph on page 8, which continues on to page 9, as follows:

~~Further, the method includes the step of forming a number of physical addresses by changing a number of the logical addresses in the range. Each logical address has a corresponding physical address. In addition, a number of the physical addresses are spaced apart (not sequential).~~ A method of adding grant information to a memory that stores information on a series of arbitration periods is disclosed in accordance with a third embodiment of the present invention. The method includes assigning a number of first addresses to a device. The number of first addresses represents a corresponding number of arbitration periods such that each first address represents one arbitration period. No two first addresses are identical. Each first address has a sequence of bits.

Please amend the first full paragraph on page 9 as follows:

~~The present invention also includes a communication circuit that includes a transmit circuit that transmits information onto a bus, and a receive circuit that receives information from the bus. The communication circuit also includes a memory that has a plurality of physical addresses where each physical address identifies an arbitration period. The plurality of physical addresses identifies a number of arbitration periods.~~ The method further includes forming a number of second addresses from the number of the first addresses such that each first address has a corresponding second address by rearranging the sequence of bits in a plurality of the number of first addresses. Each second address represents one arbitration period. No two second addresses are identical.

Please amend the second full paragraph on page 9 as follows:

~~The present invention also includes a logic circuit that is connected to the transmit circuit, the receive circuit, and the memory. If grant information is to be added to the memory, the logic circuit determines a number of desired arbitration periods requested by a communication circuit, and assigns a range of logical addresses that identify the communication circuit. The number of logical addresses in the range is equal to the number of desired arbitration periods.~~ A communications circuit is disclosed in accordance with a fourth embodiment of the present invention. The communications circuit includes a transmit circuit that transmits information onto a bus, a receive circuit that receives information from the bus, and a memory that stores information on a series of arbitration periods. The communications circuit also includes a logic circuit connected to the transmit circuit, the receive circuit, and the memory. If grant information for a group of devices is to be added to the memory, the logic circuit assigns a number of first addresses to the group of devices such that two or more consecutive first addresses are assigned to each device and no two devices have the same first addresses. The number of first addresses represents a corresponding number of arbitration periods such that each first address represents one arbitration period. Each first address has a sequence of bits.